REMARKS

In response to the Office Action mailed December 20, 2006, Applicants respectfully request reconsideration. Claims 1-7 were previously pending in this application. By this amendment, claims 1, 2, 4, 5 and 7 have been amended. New claims 8-11 have been added. As a result, claims 1-11 are pending for examination with claims 1, 7, 8 and 11 being independent. No new matter has been added.

Objections to the Specification

The Office Action objected to the specification because it contained an embeded hyperlink. Applicants have amended the specification to remove the hyperlink.

Accordingly, withdrawal of this objection is respectfully requested.

Objections to the Claims

The Office Action objected to claims 1, 2, 5 and 7 as lacking antecedent basis. Applicants have amended claims 1, 2, 4, 5 and 7 to address the Examiner's concerns.

Accordingly, withdrawal of this objection is respectfully requested.

Rejections under 35 U.S.C. §112

The Office Action rejected claim 5 under 35 U.S.C. §112 as being indefinite. Applicants have amended claim 5 to address the Examiner's concerns.

Accordingly, withdrawal of the rejection of claim 5 is respectfully requested.

Rejections Under 35 U.S.C. §103

The Office Action rejected claims 1-7 under 35 U.S.C. §103(a) as allegedly being unpatentable over Argade et al., (U.S. Patent No. 5,724,505), hereinafter Argade, in view of Nexus 5001 Forum: Standard for a Global Embedded Processor Debug Interface (The Nexus 5001 Forum), hereinafter Nexus. Applicants respectfully disagree. In addition, Applicants have amended claims 1 and 7 to more clearly distinguish over the cited references.

Claim 1, as amended, recites:

A method for transmitting digital messages, on execution of an instruction sequence by a microprocessor, through output terminals of a monitoring circuit integrated on the microprocessor, at least one of said digital messages being representative of characteristic data stored by the monitoring circuit on detection of a jump in the execution of an instruction sequence from an initial instruction to a destination instruction different from an instruction following the initial instruction in the instruction sequence, comprising, for the transmission of the at least one digital message, the steps of:

determining whether the jump is associated with a jump instruction of the instruction sequence for which data representative of a destination instruction address of the jump is explicitly indicated in the instruction;

if yes, assigning a first value to a first set of bits of the at least one digital message, and if not, assigning a second value to the first set of bits;

if the first set of bits is at the second value, providing an additional field comprising a second set of bits of the at least one digital message and assigning to the second set of bits a third value identifying the jump from among several types of jumps; and

transmitting the at least one digital message.
(Emphasis added).

Argade is directed to a digital microprocessor capable of on-chip real-time non-invasive tracing of the execution of program instructions via a serial interface (col. 1, lines 8-11). TBC block 50 enables on-chip real-time program tracing by recording only the minimum details about the discontinuity and conditionally executed instructions and their addresses necessary for the user to re-construct a full program trace (col. 5, lines 35-38).

Argade neither discloses nor suggests, if the first set of bits is at the second value, *providing an additional field comprising a second set of bits of the at least one digital message and assigning to the second set of bits a third value identifying the jump from among several types of jump*, as recited in claim 1. The second value is assigned to the first set of bits if the jump is not explicit.

Similarly, Nexus neither discloses nor suggests a method for transmitting digital messages, on execution of an instruction sequence by a microprocessor, through output terminals of a monitoring circuit integrated on the microprocessor, at least one of said digital messages being representative of characteristic data stored by the monitoring circuit on detection of a jump in the execution of an instruction sequence from an initial instruction to a destination instruction different from an instruction following the initial instruction in the instruction sequence, comprising, for the transmission of the at least one digital message, the steps of: determining

whether the jump is associated with a jump instruction of the instruction sequence for which data representative of a destination instruction address of the jump is explicitly indicated in the instruction; if yes, assigning a first value to a first set of bits of the at least one digital message, and if not, assigning a second value to the first set of bits; *if the first set of bits is at the second value, providing an additional field comprising a second set of bits of the at least one digital message and assigning to the second set of bits a third value identifying the jump from among several types of jumps*; and transmitting the at least one digital message, as recited in claim 1.

Accordingly, claim 1 distinguishes over Argade and Nexus, either alone or in combination.

Claims 1-6 depend from claim 1 and are allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 1-6 is respectfully requested.

Claim 7, as amended, recites:

> A device for transmitting digital messages between a monitoring circuit integrated on a microprocessor and an analysis tool via output terminals comprising:
> means of detection of a jump on execution of an instruction sequence by the microprocessor;
> means for storing data characteristic of the detected jump;
> means for determining a digital message based on the stored characteristic data, the digital message comprising a first set of bits set to a first value if the jump is associated with a jump instruction of the instruction sequence for which data representative of a destination instruction address of the jump are explicitly indicated in the instruction, and set to a second value in the opposite case; and
> means for transmitting the determined digital message;
> wherein, *when the first set of bits is set to the second value, the determination means is capable of providing an additional field in the digital message comprising a second set of bits, with the second set of bits set to a third value identifying the jump from among several jump types.*
> (Emphasis added).

As discussed above, neither Argade nor Nexus, either alone or in combination, discloses or suggests "a device for transmitting digital messages between a monitoring circuit integrated on a microprocessor and an analysis tool via output terminals comprising: means of detection of a jump on execution of an instruction sequence by the microprocessor; means for storing data characteristic of the detected jump; means for determining a digital message based on the stored characteristic data, the digital message comprising a first set of bits set to a first value if the jump is associated with a jump instruction of the instruction sequence for which data representative of

a destination instruction address of the jump are explicitly indicated in the instruction, and set to

a second value in the opposite case; and means for transmitting the determined digital message;

wherein, when the first set of bits is set to the second value, the determination means is capable

of providing an additional field in the digital message comprising a second set of bits, with the

second set of bits set to a third value identifying the jump from among several jump types," as

recited in claim 7.

Accordingly, claim 7 distinguishes over Argade and Nexus, either alone or in

combination.

Accordingly, withdrawal of the rejection of claim 7 is respectfully requested.

New Claims

New claim 8 recites:

A method for transmitting digital messages on execution of an instruction
sequence by a microprocessor, the method comprising:
detecting a jump in the execution of the instruction sequence from an
initial instruction to a jump destination instruction, wherein the jump destination
instruction is different from an instruction following the initial instruction in the
instruction sequence;
if the jump is implicit, providing an additional field in at least one digital
message transmitted on the execution of the instruction sequence by the
microprocessor, wherein the additional field includes a value identifying a type of
the implicit jump; and
transmitting the at least one digital message.

Claim 8 patentably distinguishes over Argade and Nexus, because none of these

references teaches or suggests "if the jump is implicit, providing an additional field in at least

one digital message transmitted on the execution of the instruction sequence by the

microprocessor, wherein the additional field includes a value identifying a type of the implicit

jump," as recited in claim 8.

Claims 9 and 10 depend from claim 8 and are therefore patentable for at least the same

reasons.

New claim 11 recites:

A device for transmitting digital messages to monitor operation of a
microprocessor, the device comprising:
a monitoring circuit integrated on a microprocessor for:

detecting, on execution of an instruction sequence by the microprocessor, a jump from an initial instruction to a jump destination instruction, wherein the jump destination instruction is different from an instruction following the initial instruction in the instruction sequence; and

if the jump is implicit, providing an additional field in at least one digital message transmitted on the execution of the instruction sequence by the microprocessor, wherein the additional field includes a value identifying a type of the implicit jump;

an analysis tool to reconstitute the instruction sequence based on the at least one digital message; and

at least one monitoring terminal to provide the at least one digital message from the monitoring circuit to the analysis tool.

Claim 11 patentably distinguishes over Argade and Nexus, because none of these references teaches or suggests "if the jump is implicit, providing an additional field in at least one digital message transmitted on the execution of the instruction sequence by the microprocessor, wherein the additional field includes a value identifying a type of the implicit jump," as recited in claim 11.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: May 21, 2007   Respectfully submitted,
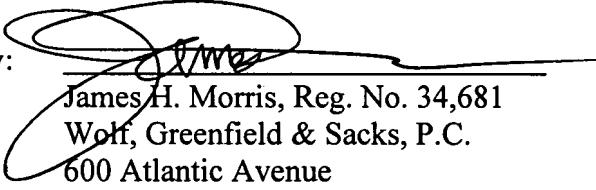
By: _____
James H. Morris, Reg. No. 34,681
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
Telephone: (617) 646-8000